Analyzing Power Integrity Issues from Power Plane Interactions

When a printed circuit board (PCB) includes a power plane that is near to signal traces or other power planes, there is a significant risk of energy transfer between parts of the system. Not only does this coupling lead to power switching noise being transferred into data signals, it also means that power supply systems may demonstrate additional resonances that are not seen in the individual components. This can affect the power integrity of the PCB and may reduce its speed or reliability. This paper will explore some of the potential power integrity issues that can affect a PCB and explain how simulation can be used to help reduce these effects.

Miniaturization and economization mean that PCB manufacturers are producing boards with high packing densities and as few layers as possible, such as the example pictured in Figure 1. In addition, modern PCBs often require several supply voltages, and therefore must include multiple power planes. This leads to circuit boards that include pairs of power planes which are not separated by ground layers, and such power planes can easily couple to each other. These effects can arise whether the planes are on the same layer or on adjacent layers.

Each power plane will have certain resonances, and the coupling to other planes can change these resonant frequencies. Since the resonances affect the impedance of the power distribution network (PDN), it is very important for the designer to consider these resonances when laying out the board.

Another common cause of power integrity issues is the use of stack-ups with signal traces running between a ground plane and a power plane. These traces can couple to the power planes as well. Not only can this change the resonances of the power planes, it also means that noise can be transferred into the data traces.

Modern complex circuit boards have many metal layers comprising thousands of signal traces, and can be very large compared to the wavelength. Simulating such a complex circuit board to identify resonances can be a challenging task, especially when taking into account all of the circuit board layers and all of the traces. Circuit simulation, representing the circuit board with R, L and C lumped elements, is not practical – building an RLC circuit to represent such a complex board is almost impossible.

EM field simulators provide a better approach, offering more accurate results than the classical technique with circuit simulators and SPICE. However, full-wave simulation needs high computational resources, and to meet the time requirements of the development cycle it is often only applied to simplified models. Often, these simplified models ignore neighboring power nets and signal traces above or below the power plane.

This paper will focus on the aforementioned effects of PDN impedance when simulating a PCB model. The first section will discuss the plane mode resonances from the test board, and the next section will focus on characterizing the coupling capacitance and the influence of neighboring power planes. Following this, the effect of signal traces on the PDN impedance will also be discussed. Finally, we will show simulation results from a real circuit board.

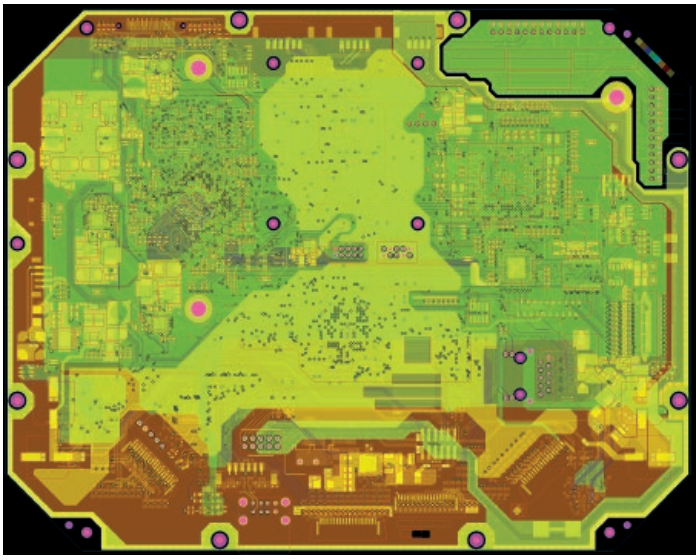

Figure 1: A complex high-speed PCB for industrial control equipment, with multiple power planes. Courtesy of Siemens

Plane resonances

One major challenge when designing a power plane is defining its dimensions, taking into account the total size of the PCB. The dimensions of the power plane determine the so-called "plane-mode" resonances, which affect PDN impedance. For a rectangular plane, the resonance frequencies can be estimated by:

$$f_{resonance} = \frac{c}{2\sqrt{\varepsilon_r}} \sqrt{\left(\frac{m}{L_x}\right)^2 + \left(\frac{n}{L_y}\right)^2} \qquad (1)$$

where c is the speed of light, L_x and L_y are the lengths in the x and y directions respectively and ε_r is the permittivity of the substrate material[1]. m and n correspond to the m-th mode in the x direction and n-th mode in the y direction.

Equation (1) holds as long as the power plane is modeled as a rectangular shape. For arbitrary shapes, it may be necessary to use a numerical method, such as the eigenmode solution, to find the plane mode resonance. The eigenmode equation is as follows:

$$\text{curl}\ \underline{\nu}\ \text{curl}\ \vec{E} = \underline{\omega}^2 \underline{\varepsilon} \vec{E} \quad (2)$$

where $\underline{\nu}$ is the complex reluctivity and $\underline{\varepsilon}$ is the complex permittivity[2]. This equation forms the basis of the eigenmode solver in CST MICROWAVE STUDIO® (CST MWS), which was used to calculate the eigenmode resonances.

For a plane with dimensions 160 mm x 70 mm and ε_r=4, the resonance frequencies from equation (1) and the eigenmode solution from equation (2) are listed in table 1.

Mode number	m	n	$f_{resonance}$ [GHz]	$f_{eigenmode}$ [GHz]
2	1	0	0.468	0.461
3	2	0	0.938	0.923
4	0	1	1.071	1.010
5	1	1	1.169	1.118
6	3	0	1.406	1.36
7	2	1	1.423	1.38

Table 1: Plane mode resonance frequencies

The first resonance frequency is related to the DC frequency, and therefore is not listed in the table.

The solution of the eigenmode equation (2) also gives the eigenvector corresponding to the specific eigenmode frequency. The field distributions based on the eigenvectors are illustrated in Figure 2.

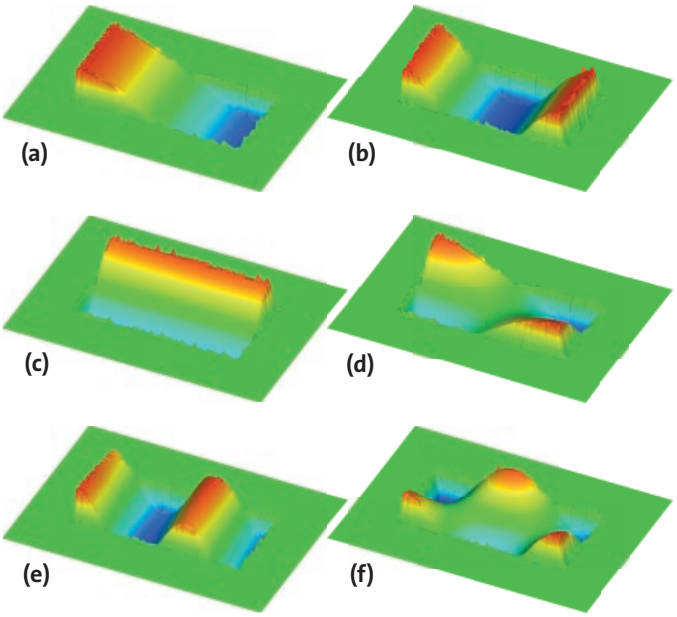

Figure 2: Spatial E-field distributions from the eigenvector
a) 2nd mode b) 3rd mode c) 4th mode d) 5th mode e) 6th mode f) 7th mode

The information from the spatial field distributions provides a good starting point for designing a power plane, as it indicates the plane mode resonances introduced when the plane is excited at the field maximums – for example, when a device is mounted there.

To characterize the plane mode resonance together with a mounted device, we cannot use the eigenmode solution, since it cannot consider passive circuit elements such as *R*, *L* and *C* in Touchstone format. Instead, we need a more advanced solver. For this, we use the 3D finite element frequency domain (FEFD) solver in CST PCB STUDIO® (CST PCBS). Using the finite element method, the 3D FEFD solver calculates the partial differential equations (PDEs) characterizing the power plane resonance.

The power and ground planes are both included in the simulation, along with the substrate material, and the model is discretized with the tetrahedral mesh. An excitation port is defined, representing a mounted device. The simulation produces an S-matrix describing the transfer function. Using a similar board to that described in Table 1, with ports defined as shown in Figure 3.

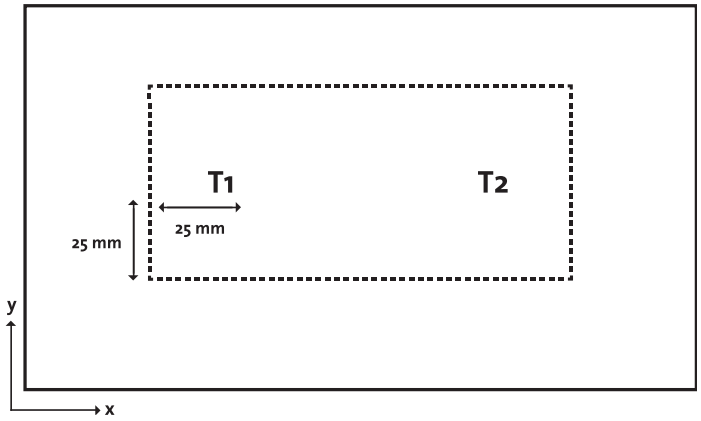

Figure 3: Port configuration for a simple test board

The three resonance frequencies correspond to the 2nd, 3rd and 9th (not listed in Table 1) resonance modes, while many other resonances are not present. This means that the resonance frequencies introduced in the impedance curve are dependent on the placement of the port.

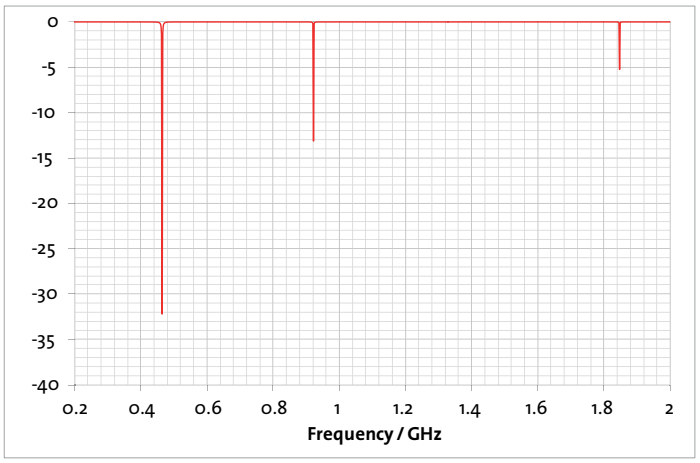

Figure 4a: S-parameter results in dB

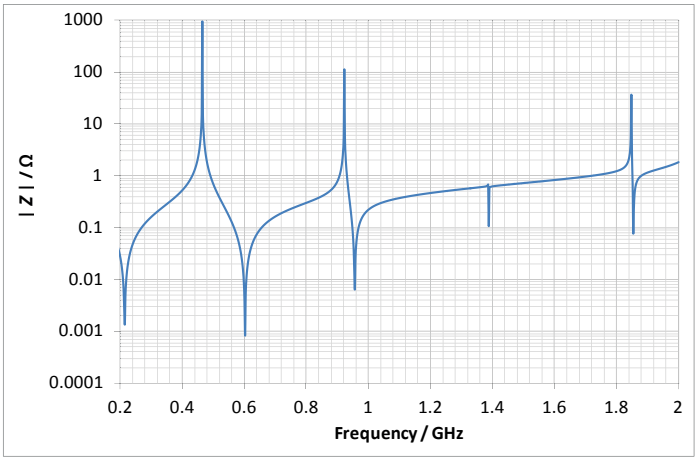

Figure 4b: Z-parameter results

Characterization of the coupling capacitance to the power distribution network

In complex circuit boards, it's quite common for there to be more than one power plane. As the thickness of the circuit board is limited, the PDN is routed over as few layers as possible. Often, a single layer will carry all the power planes.

In order to understand the effect of the interaction between the power planes, we start with a very simplified representation of two power planes on different layers using the transmission line model as illustrated below:

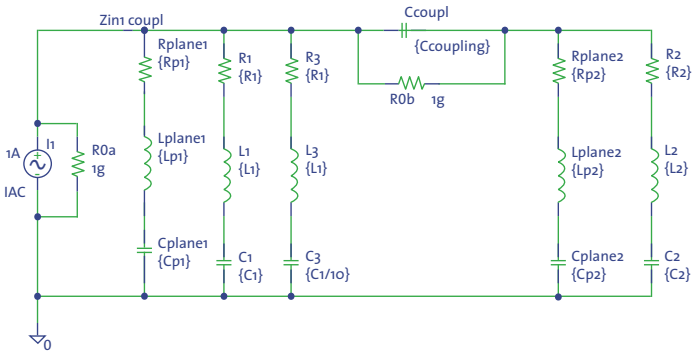

Figure 5: Circuit representation of two power planes with a capacitive coupling

Parameter	Value	Parameter	Value	Parameter	Value
R1	20 mΩ	Rp1, Rp2	20 mΩ	R2	20 mΩ
L1	1 nH	Lp1, Lp2	158 pH	L2	1 nH
C1	250 nF	Cp1, Cp2	4 nF	C2	62.5 nH

Table 2: List of parameters used in Figure 5

The parameters *Rp*1, *Lp*1 and *Cp*1 are the parasitic impedances of one of the power planes, modeled with only the first impedance minimum and no further resonances. *R*1, *L*1, *C*1 and *C*1/10 are the parasitic impedances of the two decoupling capacitors on the first power plane. Similarly, *Rp*2, *Lp*2 and *Cp*2 represent the parasitic impedances of the second power plane, and the corresponding decoupling capacitor is represented by *R*2, *L*2 and *C*2. The capacitor $C_{coupling}$ represents the coupling between the two adjacent power planes.

In general, $C_{coupling}$ can be calculated using the standard formula for the capacitance of two parallel plates[3]:

$$C_{coupling} = \varepsilon_0 \varepsilon_r \frac{A}{d} \qquad (3)$$

The distance *d* between the two planes is taken from the commonly used layer separation in a PCB stackup, which is around *100* µm. Again, ε_r is *4* and the dimensions of the power planes are *160* mm by *70* mm, which gives an area *A* of *112* cm². This gives a $C_{coupling}$ of approximately 4 nF, provided the two planes are stacked one above the other.

The value of $C_{coupling}$ is very important to the formation of resonances. As an example, Figure 6 and 7 show the impedance curves for two power planes with varying $C_{coupling}$ value calculated with CST DESIGN STUDIO™ (CST DS).

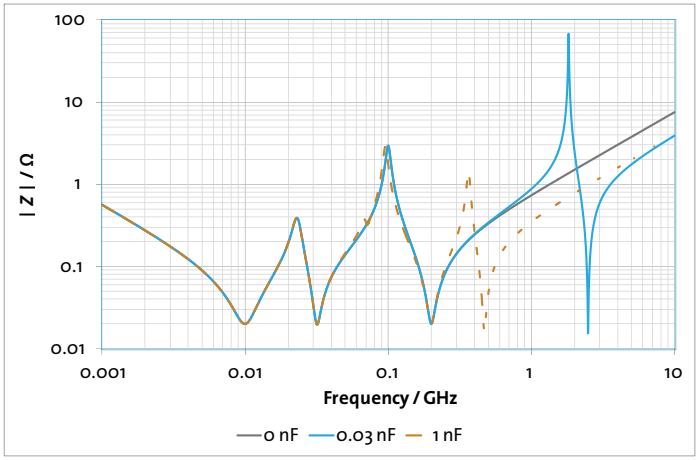

Figure 6: Impedance curve for $C_{coupling}$ = 0 nF (dotted), 30 pF (light, solid) and 1 nF (dark, dashed)

All the impedance curves show resonances around 20 MHz and 100 MHz – however, introducing even a small coupling capacitance into the system (in this case, 30 pF) causes an additional resonance to form around 1.8 GHz.

As the capacitance grows further to 4 nF, an additional resonance becomes visible at around 55 MHz, and the additional resonances get shifted towards lower frequencies. This means that when the coupling capacitance is large, the impact of the resonances at lower frequencies will be even more visible and the system will fail earlier than expected.

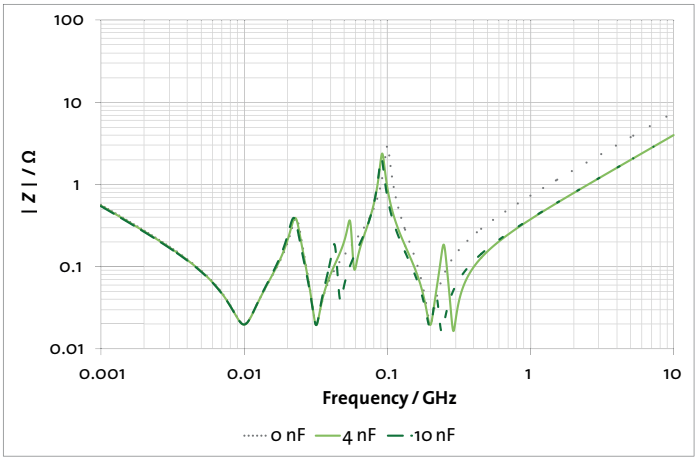

Figure 7: Impedance curve for $C_{coupling}$ = 0 nF (dotted), 4 nF (light, solid) and 10 nF (dark, dashed)

In the simple system, this lumped element approach is valid. However, although this approach may be sufficient for a preliminary study of a complex PCB, it neglects secondary effects such as via interconnections and the proximity effects between the power planes. To demonstrate the interaction between the power planes, we use two PCBs with different stackups to visualize the coupling capacitance between the PDNs.

Power planes on different layers

In this case, (Figure 8 and Table 3) the two power planes are placed on adjacent layers – here, layer 3 and layer 4 – separated by isolating material with $\varepsilon_r = 4$, with ground layers above and below. All the metal layers are copper.

Once again, the dimensions of the two power planes are 160 mm by 70 mm, with one decoupling capacitor with *R*1, L1 and *C*1 on each power plane, at opposite sides of the plane. To visualize the effect of the capacitive coupling between power planes, we vary the distance between them. A large distance of 1.5 mm is used to represent a weak coupling, and a small distance of 150 µm (common in PCB stackups) is chosen for the stronger coupling.

The board was then simulated using the power integrity (PI) solver of CST PCBS. Figure 9 shows that several new resonances appear when the distance between *P*1 and *P*2 is reduced, and as the coupling increases, the resonances shift towards lower frequencies.

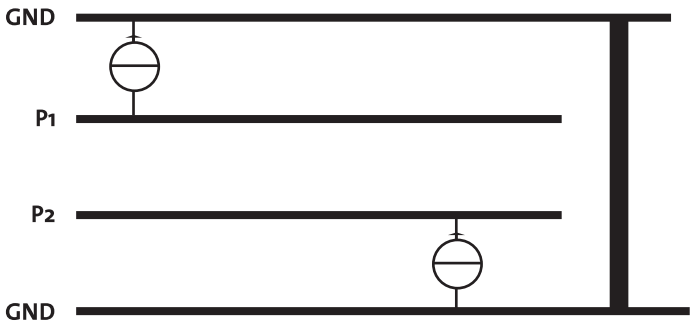

Figure 8: The cross-section of the test board

Layer Name	Type	Number	Material	Thickness (µm)
TOP GND	Signal	1	Copper	18.0
Insulator 1	Dielectric	–	FR4	75.0
Power 1	Signal	2	Copper	18.0
Insulator 2	Dielectric	–	FR4	150.0
Power 2	Signal	3	Copper	18.0
Insulator 3	Dielectric	–	FR4	75.0
BOTTOM GND	Signal	4	Copper	18.0

Table 3: Test board configuration for power planes on adjacent layers

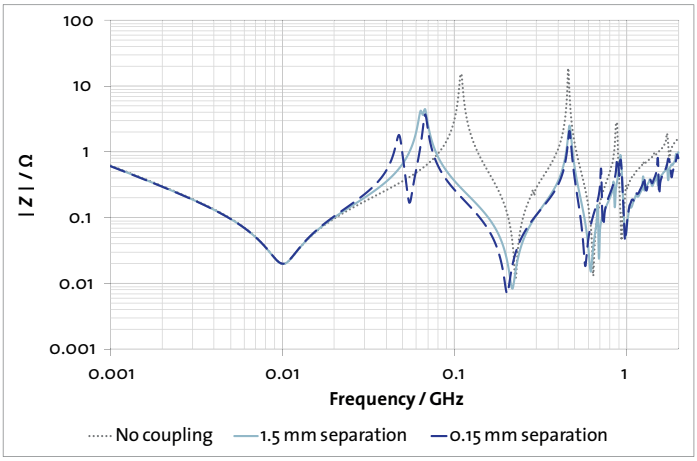

Figure 9: Impedance curves for varying distances between P1 and P2

Adjacent power planes on one layer

In many complex PCBs, the power planes are placed in the same layer, and lie side-by-side with a relatively small separation between them. Depending on the complexity of the circuit board, the distance between adjacent power planes usually varies between 100 µm and 600 µm. The thickness of the substrate layer is defined as 300 µm. An isolating layer with $\varepsilon_r = 4$ is used to separate the power planes and the bottom GND plane. One decoupling capacitor is placed 1 mm from the excitation source on each power plane, with parameters *R*1, *L*1 and *C*1. Each power plane has the dimensions 160 mm by 70 mm, and the two are placed side by side, as shown in Figure 10.

Figure 10: Test board configuration for adjacent power nets

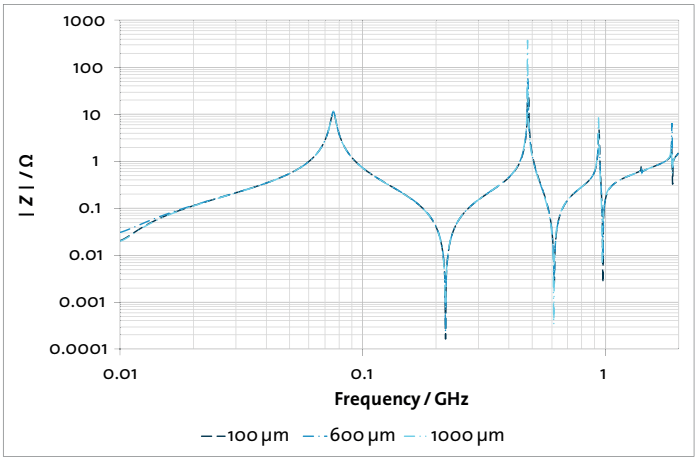

Figure 11: Impedance curves of adjacent power nets at different distances

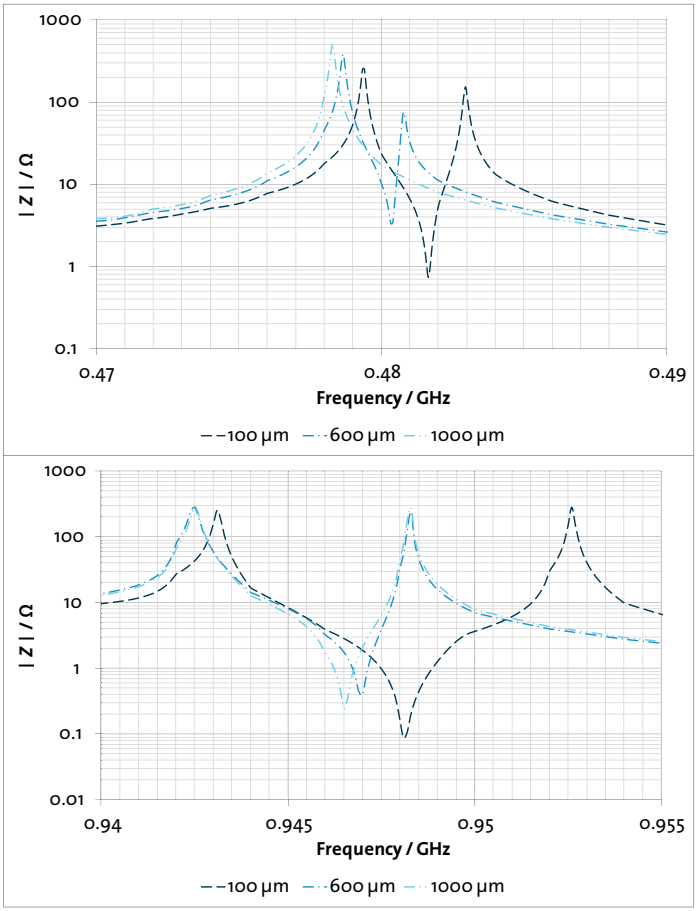

Figure 12: Close-ups of the resonance peaks at 0.48 GHz (top) and 0.94 GHz (bottom)

The corresponding impedance curves are illustrated in Figure 11 and Figure 12. Defining power planes side-by-side produces less of a negative impact on the overall impedance than defining them on adjacent layers, since the capacitive coupling happens mainly at the edges of the planes. The thickness of the metallization is usually around 10 µm, and so by equation (3), the capacitance is much smaller, being on the order of picofarads.

Resonances between planes and traces

Due to space limitations on complex PCBs, it is inevitable that some signal lines, such as the DDR data bus, will have to be routed under the power plane. Just like plane-plane couplings, trace-plane couplings can also have an impact on the resonances. To show the impact the data bus on the impedance of the power plane, we construct a virtual test circuit board, with power plane dimensions 30 mm by 50 mm (a typical size for the power plane on DDR memory). The traces are modeled with dimensions 0.1 mm by 24 mm, with a separation of 0.5 mm. The layout cross section is shown in Figure 13.

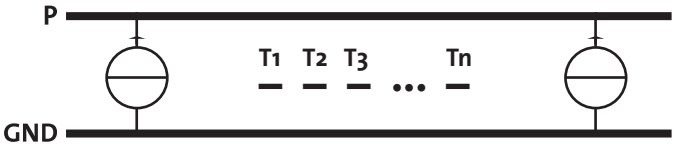

Figure 13: Test board configuration of power plane and signal traces

The power plane is located 285 µm above the ground plane, separated by a substrate with $\varepsilon_r = 4$. The signal data bus (T1, T2, ... , Tn) is located 100 µm above the ground plane. Two ports are defined between the power plane and the ground plane representing the mounted device, and two decoupling capacitors with a capacitance of 1 µF are added. Each trace has a 50 Ω termination.

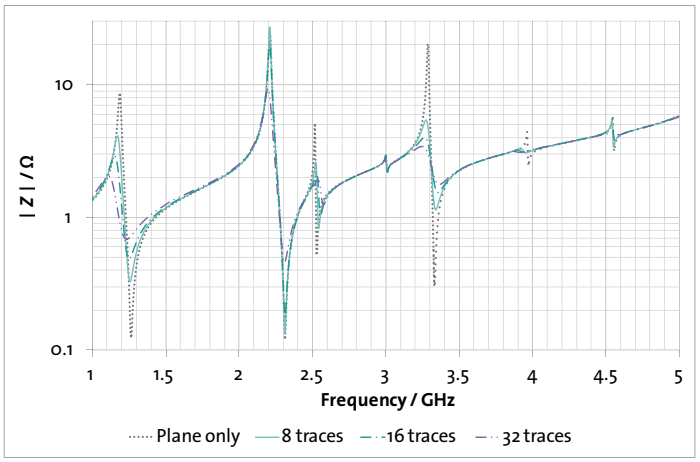

Figure 14: Impedance curve for varying numbers of signal traces

Figure 14 shows how, in contrast to the interaction between power planes, the coupling between traces and the power planes can reduce the impedance magnitude at higher frequencies without introducing additional resonances. Increasing the number of

signal traces improves the impedance profile further. This can only works if the signal traces are terminated, however. The termination absorbs the RF energy coupling into the trace and converts it into heat.

Floating (unterminated) signal traces on the other hand have no impact on the impedance result, since the field coupling into them is not absorbed (Figure 15). This also means that the traces act as radiators, which can lead to EMC problems.

These results hold as long the excitation of the power plane is located far enough away from the signal traces. When the traces are close to the excitation, they can introduce additional power plane resonances.

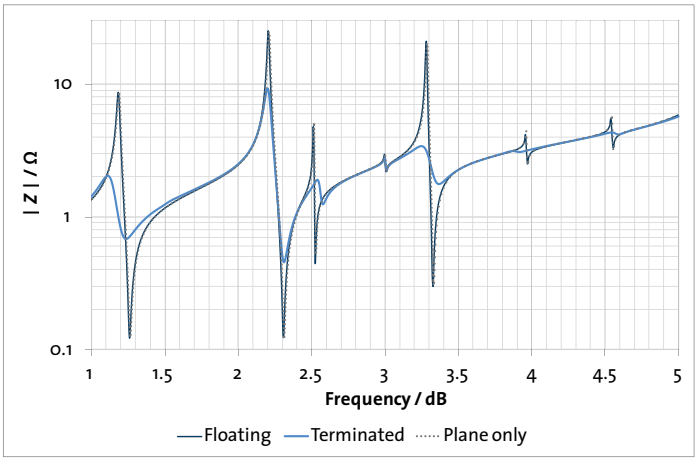

Figure 15: Impedance curve for a board with 32 signal traces, comparing terminated and floating conditions

Practical examples

In this section, we will use the techniques discussed to simulate a real circuit board design, consisting of 8 metal layers, with a total thickness of 1.68 mm. The layer stackup is shown in Table 4. This board is part of a handheld terminal for operating industrial production machinery, provided by Siemens, and includes an LCD display and several control elements.

Layer Name	Type	Number	Material	Thickness (µm)
SOLDER_MA...	Signal	–	Solder-Mask	40
1	Dielectric	1	Copper	44
Substrate-1	Signal	–	FR4	75
2	Dielectric	2	Copper	15
Substrate-2	Signal	–	FR4	100
3	Dielectric	3	Copper	15
Substrate-3	Signal	–	FR4	185
4	Signal	4	Copper	15
Substrate-4	Dielectric	–	FR4	710
5	Signal	5	Copper	15
Substrate-5	Dielectric	–	FR4	185
6	Signal	6	Copper	15
Substrate-6	Dielectric	–	FR4	100
7	Signal	7	Copper	50
Substrate-7	Dielectric	–	FR4	75
8	Signal	8	Copper	44
SOLDER_MA...	Dielectric	–	Solder-Mask	40

Table 4: Layer stackup

The ground planes are located on layers 1, 2 and 7, while the power planes are located on layers 4 and 5 (Figure 17). The power plane on layer 4 is referenced to the ground plane on layer 2, and the power plane on layer 5 is referenced to the ground plane on layer 7.

Five different power nets are defined on the fourth layers and seven power nets are defined on the fifth layer. The dashed white line marks the area of interest, covering the power net P3V3_S on layer 4. For the impedance calculation, we select one test point from the circuit component mounted on this power net. The board is simulated with the PI solver to calculate its impedance profile.

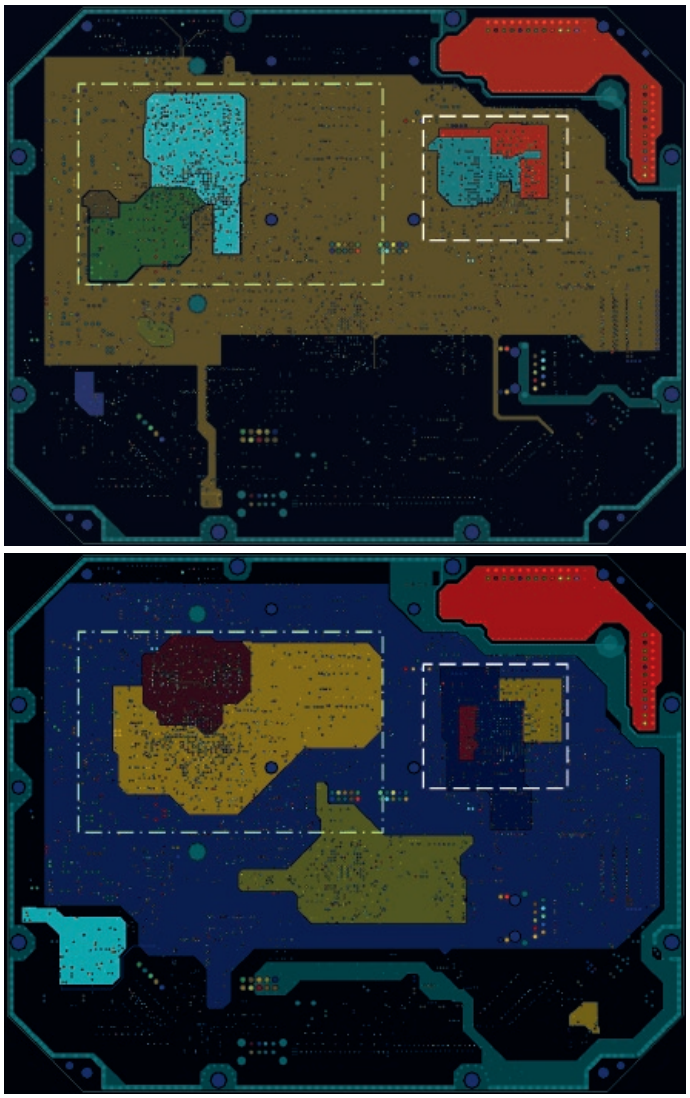

Figure 17: Power planes on the fourth and fifth layers

The second area of interest, marked with the green dashed-dotted line, shows a large overlapping area, which means a larger capacitive coupling. The power net P1V05 is defined in this area on layer 5. The planes were simulated in isolation (no coupling) and taking neighboring nets into account (with coupling).

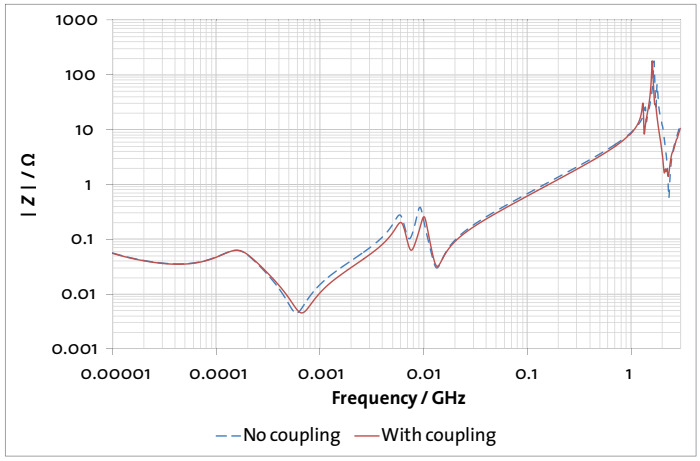

Figure 18: Impedance curve of power net P3V3_S

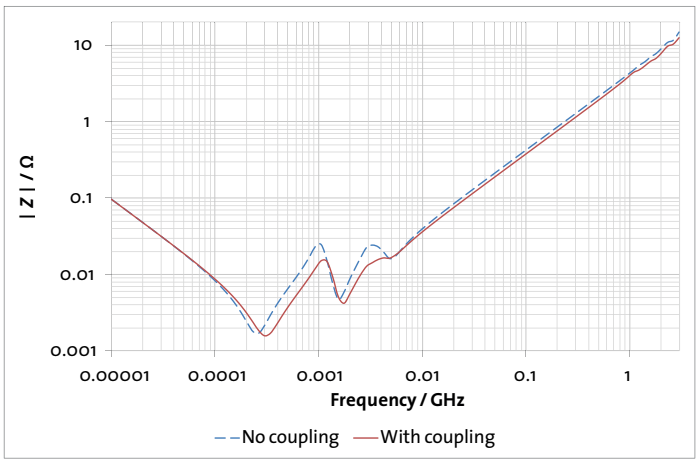

Figure 19: Impedance curve of power net P1V05

The effect of this overlap can be seen by comparing Figure 18 and Figure 19. This overlap causes a capacitive coupling between the power nets and as expected, the stronger coupling experienced by P1V05 tends to shift the resonant frequencies down, and can lead to additional resonances at higher frequencies. The effects are still relatively small, since decoupling capacitors have been included to reduce the resonances.

The next example shows the influence of the signal traces to the impedance of the power plane, as discussed earlier. Figure 21 illustrates the power plane P1V8, along with the 32 DDR data lines DQ[0], ... , DQ[31] and the 16 address input lines MA[0], ... , MA[15] located on layer 3, all with 50 Ω terminations.

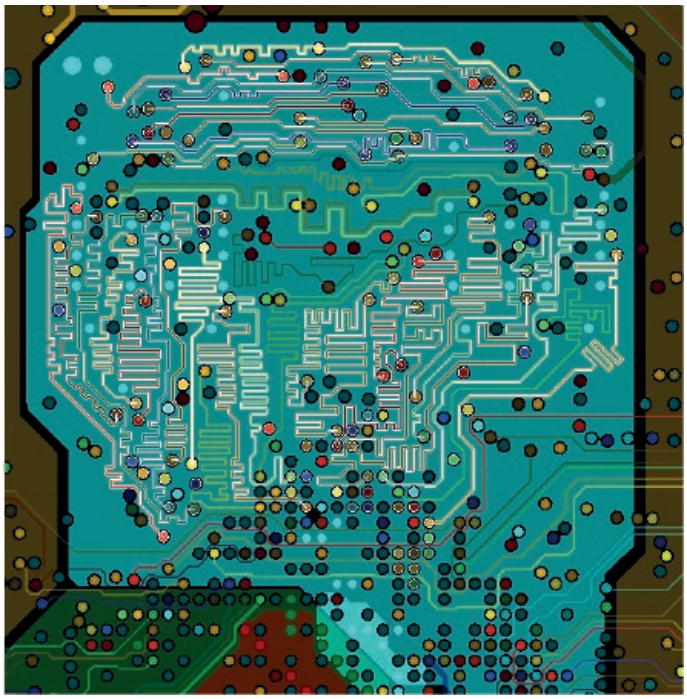

Figure 21: Power net P1V8 (green), with 32 DQ and 16 MA lines (highlighted)

Figure 22 shows similar behavior to that seen on the test board. Although the fine detail of the traces made the simulation more computationally demanding, a significant effect was shown when they were included in the calculation. This will mean that for accurate prediction of resonant frequencies of power planes, the signal traces should be considered since the overall impedance will be affected.

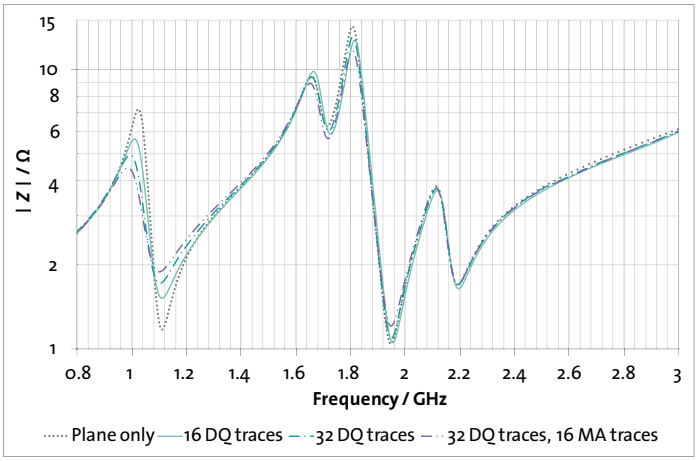

Figure 22: Impedance curve comparison for different number of DQ-lines

Conclusions

This paper has briefly summarized the most important issues when trying to design and simulate the power distribution network for a high-speed system with power integrity in mind.

It has been demonstrated how attempting to simplify the simulation by neglecting the role of signal traces or power planes can lead to different impedances. We have also shown that routing signal traces above or below the power planes can improve the impedance profile, as long as the traces are terminated.

When dealing with power plane resonances, it is important to define power planes side-by-side rather than on adjacent layers, wherever practical. If it is impossible, the coupling effect can be reduced by using a thicker core or substrate the separate the layers. Reducing the size of the power plane can also help, since it reduces the overlapping area between the planes.

[1] Takashi Harada, Hideki Sasaki and Yoshio Kami, "Controlling Power-Distribution-Plane Resonance in Multilayer Printed Circuit Boards", IEICE Trans. Commun., Vol.E83-B, No.3 March 2000.

[2] CST STUDIO SUITE®2012, www.cst.com

[3] Yukihiro Fukumoto, "EMC Design Method for Suppressing Power Ground Noise of Digital Printed Circuit Boards", Doctoral Thesis, Appendix A "Resonance of Power and Ground Plane of PCB", pp. 83-92, March 2001

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