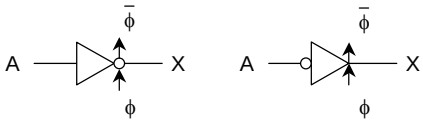
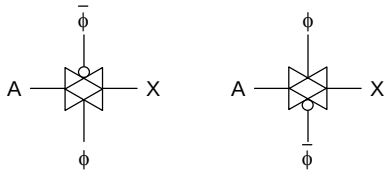
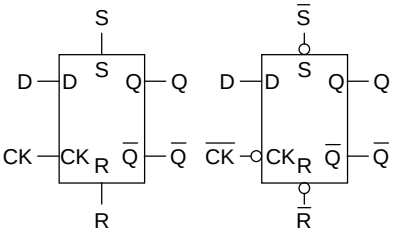
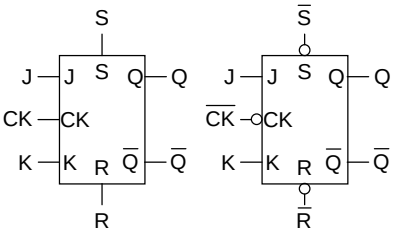
[4] Logic Symbols and Truth Table

1. How to Read MIL-Type Logic Symbols

Table 1.1 shows the MIL-type logic symbols used for high-speed CMOS ICs. This logic chart is based on MIL-STD-806. The clocked inverter and transmission gates have specific symbols.

Table 1.1 MIL Logic Symbols

Circuit Function	Logic Symbols	Logic Equation or truth Table
Inverter		$X = \overline{A}$
NAND Gate		$X = \overline{A \cdot B} = \overline{A} + \overline{B}$
NOR Gate		$X = \overline{A + B} = \overline{A} \cdot \overline{B}$
AND Gate		$X = A \cdot B = \overline{\overline{A} + \overline{B}}$
OR Gate		$X = A + B = \overline{\overline{A} \cdot \overline{B}}$
Clocked inverter (Note 1)		ϕ | A | X H | H | L H | L | H L | X | Z X : Don't care Z : High Impedance
Transmission gate (Note 2)		ϕ | A | X H | H | H H | L | L L | X | Z X : Don't care Z : High iImpedance

<table>
<tr><th>Circuit Function</th><th>Logic Symbols</th><th>Logic Equation or truth Table</th></tr>
<tr><td>Exclusive-OR Gate</td><td> 
</td><td>$X = (A + B)\cdot(\overline{A} + \overline{B})$</td></tr>
<tr><td>Exclusive -NOR Gate</td><td> 
</td><td>$X = (A\cdot B) + (\overline{A}\cdot\overline{B})$</td></tr>
<tr><td>D-Type flip-flop</td><td> 
</td><td>
<table>
<tr><th>S</th><th>R</th><th>D</th><th>CK</th><th>Q</th></tr>
<tr><td>H</td><td>L</td><td>X</td><td>X</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>X</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>↑</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>↑</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>↓</td><td>Qn△</td></tr>
</table>
X : Don’t care
△ : No change
</td></tr>
<tr><td>J-K flip-flop</td><td> 
</td><td>
<table>
<tr><th>S</th><th>R</th><th>J</th><th>K</th><th>CK</th><th>Q</th></tr>
<tr><td>H</td><td>L</td><td>X</td><td>X</td><td>X</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>X</td><td>X</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>↑</td><td>Qn△</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>↑</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>↑</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>↑</td><td>Qn▽</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>X</td><td>↓</td><td>Qn△</td></tr>
</table>
X : Don’t care
△ : No change
▽ : Toggle
</td></tr>
</table>

Note1: Clocked Inverter

The clocked inverter circuit is shown in Figure 1.1. In this figure, Q1 and Q2 are P-channel MOSFETs, and Q3 and Q4 are N-channel MOSFETs.

The four FETs are connected in series from V_{CC} to GND.

If the ϕsignal is High Q1 and Q4 turn on, and the circuit can be regarded as simply an inverter composed of Q2 and Q3. When the ϕsignal is Low, both Q1 and Q4 turn off, regardless of the condition of the A input. The output, X, is cut off from both V_{CC} and GND and is thus set to High Impedance.

Thus, a clocked inverter can be used as a switch to isolate the output from the input.

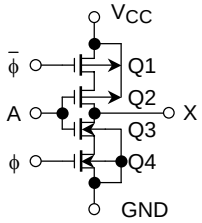


Figure 1.1 Clocked Inverter

Note2: Transmission Gate

The transmission gate circuit is shown in . in Figure 1.2.

As shown in this figure, Q1 is a P-channel MOSFET and Q2 is an N-channel MOSFET; these are connected in parallel. If the ϕ signal is High, both Q1 and Q2 turn on, and a signal can be applied in either direction. If ϕ is Low, both Q1 and Q2 turn off, and no signal can pass.

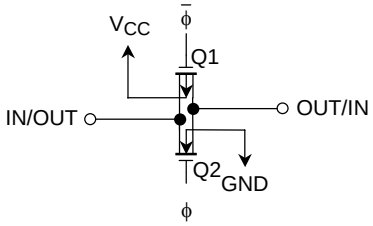


Figure 1.2 Transmission Gate

2. How to Read a Truth Table

Table2.1 explains the symbols used in truth tables.

Table 2.1 Explanation of Truth Table

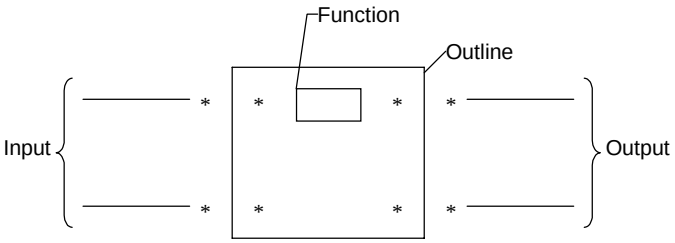
Symbol	Definition
H	High level (indicates stationary input or output)
L	Low level (indicates stationary input or output)
	Indicates leading edge
	Indicates trailing edge
X	Don't Care (either H or L)
Z	High Impedance state
a·····h	Stationary input level of inputs a to h
Q_0	Level of Q just before realization of input condition indicated in truth table
Qn	Level of Q just before input of active edge ( or )
	One H level pulse
	One L level pulse

3. Explanation of IEC Logic Symbols

(1) Logic symbol composition

A logic symbol consist of an outline, a descriptive symbol, input/output lines and various additional information. The descriptive symbol indicates the operation of the device. These are classified into the following three types: function symbols, which indicate the logic function of the device; input and output symbols, which indicate input and output connections and logic states; and internal connection symbols.

The additional information relates to specific inputs/outputs not specified under this standard and information regarding the general logic functions of the device. Additional information is shown within the outline enclosed in brackets [ ].



*: Qualifying Symbols for inputs and outputs

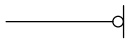
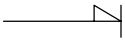
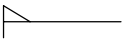
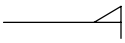
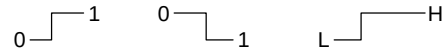
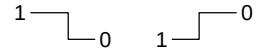
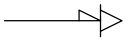
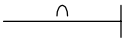
(2) Qualifying Symbols

(a) Function Qualifying Symbols

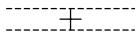
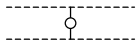
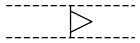
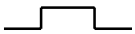
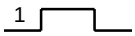
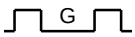
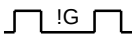
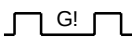
Symbol	Definition
&	AND element
≥ 1	OR element
= 1	Exclusive OR element
=	Logic identify element. If all inputs have the same logic state, then the output is at internal logic 1.
2 K	Even element. If an even number of inputs are at internal logic 1, then the output is at internal logic 1.
2 K + 1	Odd element. If an odd number of inputs are at internal logic 1, then the output is at internal logic 1.
1	Odd element. If an odd number of inputs are at internal logic 1, then the output is at internal logic 1.
▷ or ◁	Buffer element with amplified output. The triangle points in the direction of signal flow.

(b) Input and Output Qualifying Symbols

The input and output symbols indicate function and characteristic information relating to inputs, outputs and other connections.

Symbol	Definition
	Logical negation at an input. An external logic 0 (1) produces an internal logic 1 (0).
	Logical negation at an output. An internal logic 0 (1) produces an external logic 1 (0).
	Polarity indicator at an input. A L (Low) level active.
	Polarity indicator at an output. A L level active.
	Polarity indicator at an input where the signal flow is from right to left
	Polarity indicator at an output where the signal flow is from right to left
	Indicator for direction of signal flow
	Bidirectional information flow (alternate)
	Dynamic input Positive logic Negative logic Polarity  The above transitions set the internal logic to active.
	Dynamic input Positive logic Negative logic  The above transitions set the internal logic to active.
	Dynamic input Positive logic  The above transitions set the internal logic to active.
	Non-logic connection
	Input for analog signals

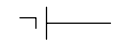
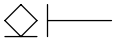
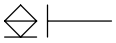
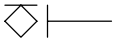
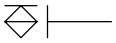
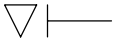
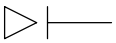
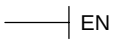
(c) Symbols for Internal Connections

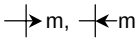
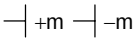
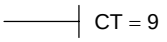
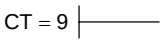
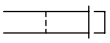
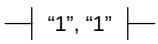
Symbol	Definition
	A logic 1 on the left-hand side produces a logic 0 on the right-hand side.
	Negated internal connection. A logic 1 on the left-hand side produces a logic 0 on the right-hand side.
	Dynamic internal connection. A transition from internal logic 0 to internal logic 1 on the left-hand side produces a transitory logic 1 on the right-hand side.
	Internal input (virtual). This input is always at internal logic 1 unless overridden or modified.
	Internal output (virtual). This effect on the internal input connected to this output must be indicated using dependency notation.
	Schmitt-trigger This has hysteresis characteristics.
	Retriggerable monostable element
	Non-retriggerable monostable element
	Unstable element
	Synchronous-starting unstable element
	Synchronous-stopping unstable element
SRGm	Shift register. m: number of bits
CTRm	Binary counter. m: number of bits, cycle length: 2
CTRDIVm	Counter of cycle length m
RCTRm	Ripple carry counter. m: number of bits, cycle length: 2
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used.
MUX	Multiplexer / data selector
DMUX or DX	Demultiplexer
Σ	Adder
P-Q	Subtracter
CPG	Look-ahead carry generator
π	Multiplier

Symbol	Definition
COMP	Comparator
ALU	Arithmetic logic unit
ROM	Read-only memory
RAM	Random access memory
FIFO	First-in first out memory
I = 0	When power is switched ON, the element goes to internal logic 0.
I = 1	When power is switched ON, the element goes to internal logic 1.
	Delay element with specified delay times When the input state changes from 0 to 1, the output state changes accordingly after a delay of t1. When the input state changes from 1 to 0, the output state changes accordingly after a delay of t2.

(d) Symbols inside the Outline

These symbols are used inside the outline. They specify input/output characteristics and functions.

Symbol	Definition
	Delayed output. The output change is delayed until the input that caused the change returns to its initial external state or level.
	Schmitt trigger input
	Open-drain output without internal pull-up resistor
	Open-drain output with internal pull-up resistor
	Open-source output without internal pull-down resistor
	Open-source output with internal pull-down resistor
	Three-state output
	Buffered output. (The triangle points in the direction of signal flow.)
	Enable input
J, K	JK Flip-Flop Inputs

Symbol	Definition
R, S	Reset, Set, Trigger and control flip-flop inputs
T	T-input (clock) for trigger (toggle) flip-flop The output state is inverted every time the input is set to 1.
D	D-input (data) for D-type flip-flop The input state is held in memory for a certain period. This symbol requires subordinate notation.
	Shift input. The direction of shifting is to the right or the left, as shown by the arrow. m = 1, 2, 3... ; however, the number may be omitted when
	Counting input. Count-up or count-down are indicated by + and - respectively. The number m is the count per command and may be omitted when m = 1.
	Bit-grouping symbol. m is the highest power of 2 in the group.
	Content input. Internal logic 1 sets the element to the value m.
	Content output. For example, when the input state is 1, the internal register is set to 9.
	Line-grouping symbol. The inputs enclosed by this symbol form a single logic input.
	Fixed-mode input. Fixed-state output. This input (or output) is permanently at internal logic 1.

(3) Dependency Notation

Dependency notation is the powerful tool that makes IEC logic symbols compact and yet meaningful. With IEC symbols, the relationships between inputs and outputs are clearly illustrated without the necessity for showing all the elements and interconnections involved.

In dependency notation, the terms “affecting” and “affected” are used.

(a) The General Rules of Dependency Notation

1) An input (or output) affecting other inputs or outputs is labeled with a letter symbol that indicates the relationship involved, followed by an appropriate identifying number.
2) Each input or output affected by that affecting input (or output) is labeled with the same number.
3) If the complement of the input's (or output's) internal logic state affects inputs or outputs, then a bar is placed over the identifying numbers of the affected inputs or outputs.
4) If the affected input or output has a label to denote its function, this label will have the identifying number of the affecting input as a prefix.
5) If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together.
6) If the labels denoting the function of affected inputs or outputs are numbers (e.g. outputs from a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g. a Greek letter.
7) If an input or output is affected by more than one affecting input, the identifying numbers of all the affecting inputs, separated by commas, will appear in the label of the affected input (or output). The normal reading order of these numbers is the same as the sequence of the affecting relationships.

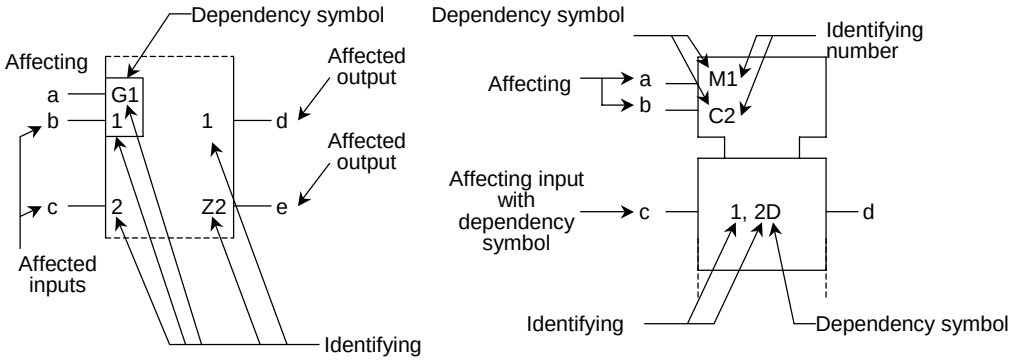


Figure 3.1 Example of Dependency Notation

(b) Symbols for Dependency Notation

Function	Symbol	Input State 1	Input State 0
AND	G	Permits action	Imposes 0 state
OR	V	Imposes 1 state	Permits action
Negate (EX-OR)	N	Complements state	No effect
Interconnection	Z	Imposes action	Permits action
Control	C	Permits action	Prevents action
Set	S	S = 1, R = 0	Prevents action
Reset	R	S = 0, R = 1	Prevents action
Enable	EN	Permits action	Prevents action of input
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Address	A	Permits action (address selected)	Preventsaction (address not selected)